EXHIBIT 5

Filed: April 25, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2022-00237
Patent 10,268,608 B2

PATENT OWNER'S PRELIMINARY RESPONSE UNDER 35 U.S.C. § 313 AND 37 C.F.R. § 42.107

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I. INTRODUCTION

Netlist, Inc. ("Patent Owner") submits this Preliminary Response to the Petition ("Petition" or "Pet.") of Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC ("Petitioners") seeking *inter partes* review ("IPR") of U.S. Patent No. 10,268,608 ("the '608 Patent").

The Board should deny institution because Petitioners failed to meet their burden of establishing that any of the claims of the '608 Patent are rendered obvious by the proposed combinations. Specifically, in all three Grounds, Petitioners failed to show that either Osanai or Tokuhiro discloses the claimed "*delay circuit configured to delay a signal through the data path . . . in response to at least one of the module control signals*" limitation.

Additionally, the Board should deny the Petition pursuant to *Apple Inc. v. Fintiv, Inc.*, Case IPR2020-00019, Paper 11 (P.T.A.B., Mar. 20, 2020) ("*Fintiv I*") (precedential). By the time the Board enters a final written decision in this proceeding, significant resources will have been spent by both parties to prepare for trial in the parallel district court action. To prevent duplicative proceedings and to promote efficiency, the Board should exercise its discretion and deny institution under 35 U.S.C. § 314(a), 37 C.F.R. § 42.108(a), and 35 U.S.C. § 316(b).

II. TECHNOLOGICAL BACKGROUND

A. The '608 Patent

The '608 patent was filed on November 21, 2017 and is a continuation of U.S. Patent No. 9,824,035, which claims priority to U.S. Provisional Patent Application No. 61/676,883, filed on July 27, 2012. It generally relates to memory modules, and more particularly to multi-rank memory modules and methods of operation.

For example, the '608 Patent discloses an embodiment of the invention including a module control device 116, a plurality of buffer circuits 118, and memory devices 12 that are mounted on the memory module 110. Ex. 1001 at 4:18-25. The module control device 116 receives command and address signals from the system memory controller 101. *Id.*, 4:65-5:10. The module control device 116 outputs module command signals and module control signals to the memory devices and the buffer circuits, respectively. *Id.*, 5:57-6:3. The module control device 116 also receives a system clock signal and outputs a module clock signal to the memory devices 12 and buffer circuits 118. *Id.*, cl. 1.

The specification also discloses that buffer circuits 118 include a command processing circuit 640 that provides processed, decoded, and processed module control signals to routing circuits. *Id.*, 12:3-26. Buffer circuits 118 also include a delay circuit that is configured to delay a signal through the data path by an amount

determined by the command processing circuit in response to at least one of the module control signals. *Id.*, cl. 1.

Figure 2A shows the logical interconnection of these components of an embodiment, while Figure 2C shows the physical arrangement of the same components on the module.

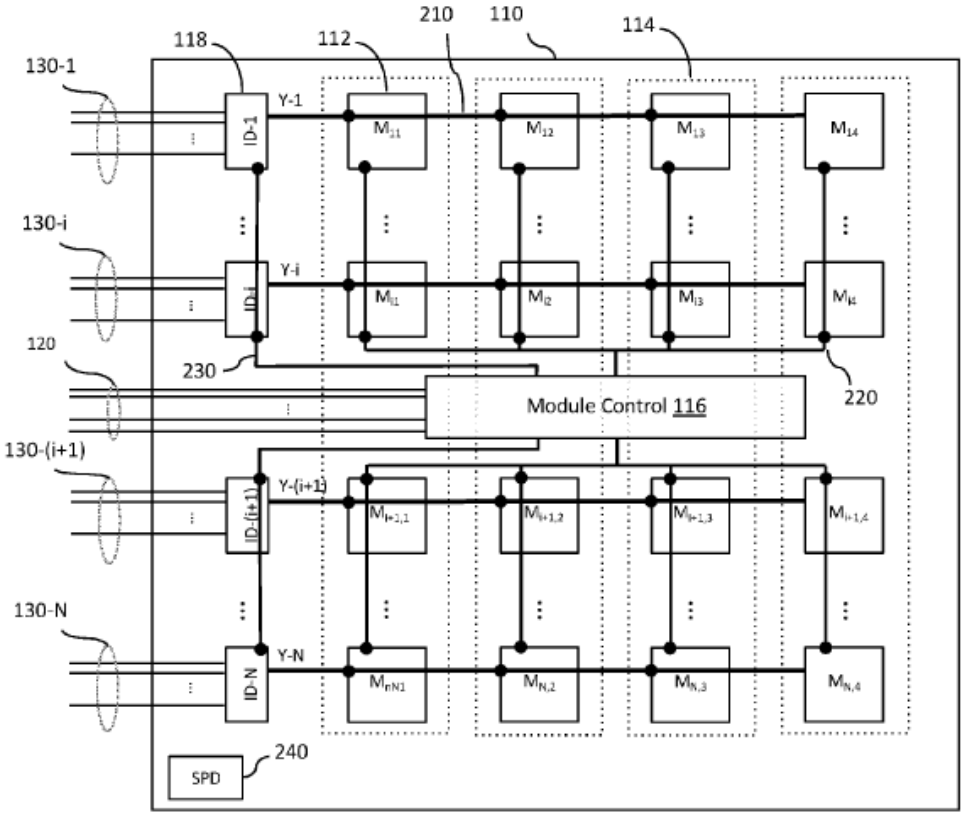


FIG. 2A

Id., Fig. 2A.

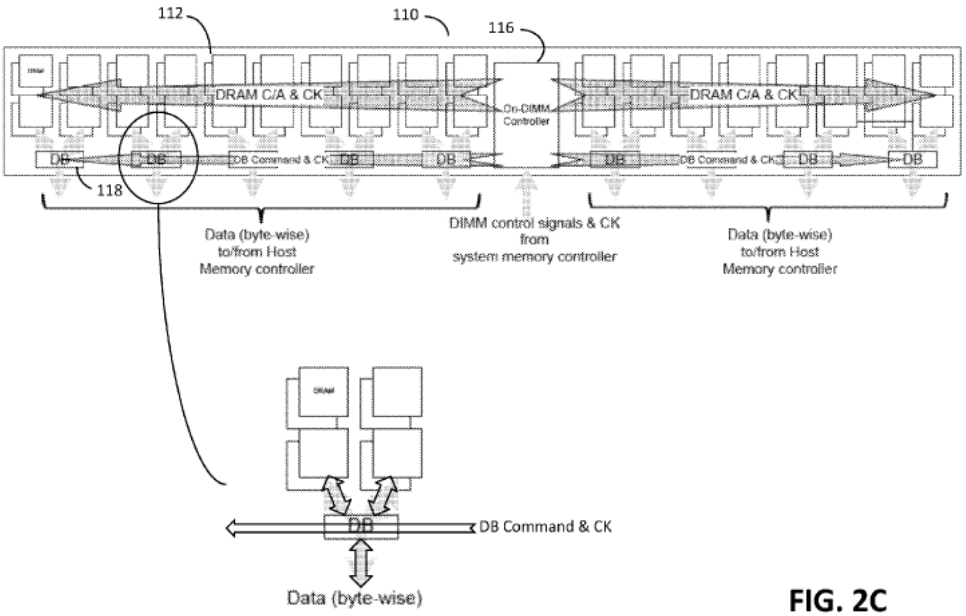


FIG. 2C

Id., Fig. 2C.

The '608 Patent describes the need to overcome limitations of prior art memory modules and the complications posed by increasing the number of memory devices—and thus the memory density—on the memory module. For example, the specification describes the limitations of conventional read and write leveling mechanisms that were known in the prior art and used to compensate for unbalanced wire lengths:

> In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

Id., 2:20-27.

Thus, the embodiments of the '608 Patent present mechanisms for buffering command, address, timing, and data information via a module control device, a plurality of buffer circuits, and memory devices located on the memory module, resulting in modules with higher capacity and higher performance. Specifically, the '608 Patent discloses that the buffer circuits 118 include a data path that includes a delay circuit that is configured to delay a signal through the data path by an amount determined by the command processing circuit in response to module control signals. *Id.*, cl. 1.

B. The Osanai Reference (Ex. 1005)

Osanai is directed to a "Load Reduced memory module in which a considerably high data transfer rate can be realized" by including a plurality of data register buffers, data connectors, and memory chips in a line along a memory module substrate. Ex. 1005, [0008], [0018]. In this way, "a line length from a data connector to a memory chip is considerably shortened," which "makes it possible to enhance the signal quality on the module substrate." *Id.*, [0018].

The components on the disclosed memory module 100, shown in Figure 1, include the register buffer 400, the buffers 300, and the memory chips 200. *Id.*, Fig. 1. The singular command/address/control register 400, shown in more detail in Figure 6, receives commands sent by the memory controller 12 over signal paths 23

(also called line L3). *Id.*, [0074-75], [0109], [0113], Figs. 1, 3, 6, 7. From these commands, the register device 400 generates control signals directed to the buffer circuits 200 and the memory devices 200. *Id.*, Figs. 1, 6. These exit the register device through ports 403 and 402 respectively and traverse the module to reach the memory devices 200 and their corresponding data register buffers 300. *Id.*, [0120], [0113], Figs. 1, 7.

Osanai's data register buffers 300 receive data flowing from the off-module memory controller (write data) to the memory chips 200 and data flowing from the memory chips to the off-module memory controller. *Id.*, [0090-99], Fig. 5. In both directions, the data is forwarded to the opposite interface and transmitted towards its destination. *Id.* In Osanai's modules, the data signals (labelled DQ) are paralleled by a strobe signal (called DQS). *Id.*, [90].

Osanai describes read and write leveling operations to adjust write timing or read timing "in consideration of a propagation time of a signal." *Id.*, [0146]. As disclosed in Osanai, write leveling operation is performed by the write leveling circuit 322 to match the phase of the strobe signal DQS to the clock signal CK. Because it takes a certain amount of propagation time until the DQS reaches Osanai's memory chip 200, then the input timing of the clock signal CK and the strobe signal DQS are not always the same. The clock signal CK is supplied from

the command/address/control register buffer 400 to both of Osanai's data register buffer 300 and the memory chip 200. *Id.*, [0148-49].

Specifically, Osanai sends a strobe signal DQS to memory chip 200 and in response to a logical "High level" of the clock signal CK at a rising edge of the strobe signal DQS, the memory chip 200 outputs a "High level" signal back to the data register buffer 300 using a DQ input of the data register buffer 300, by which the data register 300 can find a direction of phase shift between the clock signal CK and the data strobe signal DQS. Upon completing the write leveling the phases (timing) of the clock signal CK and the strobe signal DQS input to the memory chip 200 are substantially matched with each other. *Id.*, [0150-52], Figs. 14A and 14B. Consequently, Osanai's "timing adjustment" obtained from write leveling operation is to make the strobe signal DQS arrive at the memory chip 200 substantially at the same time as when the clock signal CK arrives at the memory chip 200.

The read leveling operation in Osanai determines when *e.g.*, the input buffers INB are activated, *i.e.*, turned on, to receive data signals and strobe signals coming from the SDRAMs over L1 and L2 via terminals 341, 342, 351, and 352. *Id.*, [0146], [0153-57], Fig. 15.

> The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is

> … used in an adjustment of an activation timing of the input buffer circuit INB and the like.

Id., [0157].

Osanai's data register control circuit 320 controls operations of an input buffer INB and an output buffer OUTB by generating buffer control signals, including buffer control signal BC, and at the same time, controls operations of selectors 331 to 334 by generating a select signal SEL. *Id.*, [0094]. Consequently, Osanai's "timing adjustment" of when to turn on the input buffer INB does not delay any signal going through the input buffer INB.

Furthermore, Osanai does not disclose that any "timing adjustment" made by write leveling circuit 322 or read leveling circuit 323 is made during any memory operation.

C. The Tokuhiro Reference (Ex. 1006)

Tokuhiro discloses a system that detects time delays during known write leveling procedures and applies such delays to adjust strobe signals sent from the system memory controller to a memory module during a write operation. Ex. 1006, 3:16-26, 2:10-23. In this way, Tokuhiro describes that the strobe signals will arrive at substantially the same time as the clock signal sent from the system memory controller at respective SDRAMs of the memory module. *Id.* at 2:39-45, 12:59-63. Due to lack of compensation for signal arrival time during read operation, Tokuhiro proposed an improved system whereby such time delays detected for the strobe

signals during write leveling could be used to compute similar adjustments for signals received from respective SDRAMs of the memory module during a *read operation*. *Id.* at 2:54-59, 13:66-14:6, equations (1), (2-1)-(2-3), (3-1)-(3-6). Tokuhiro discloses a fly-by topology for wiring between the memory controller 12 and the SDRAM devices mounted on DIMM module 11. *Id.* at 5:24-30.

Importantly, Tokuhiro describes and incorporates known write leveling mechanisms, as disclosed in the Joint Electron Device Engineering Counsel ("JEDEC") DDR3 SDRAM Standard, JESD79-3. *Id.*, 1:22-32; 2:10-12; 2:46-49; 2:54-59. The specification describes that:

> The term "write leveling function" refers to the function of sampling the clock signal CK by using the data strobe signal DQS output from the memory controller 90, detecting the phase relationship between the data strobe signal DQS and the clock signal CK, and adjusting (compensating) a delay time of the data strobe signal DQS.

Ex. 1006, 2:13-18.

In this way, "the difference in the delay time caused in the write operations between the memory controller . . . and the plurality of SDRAMS . . . is adjusted by employing the write leveling function." Tokuhiro noted that, although such the JEDEC DDR3 standards specified such write leveling procedures for write operations, "compensations of the signal arrival time in read operations are not provided with the JEDEC standards." *Id.*, 2:54-59.

Accordingly, Tokuhiro's system disclosure focuses on computing time delays for compensating signals during read operations using detected delays by the well-known write leveling function. Tokuhiro's first delay time control unit 23 and second delay time control unit 24 are located on the CPU 13, while the variable delay circuits are part of the control circuit units on the memory controller 12. *See id.* at Fig. 4.

Tokuhiro acknowledges that the write leveling function and variable delay circuits which can change respective delay times of the data strobe signals are present in the prior art and that their use in a system memory controller is also not novel. *Id.*, 2:19-23, 1:34-2:49, Fig 2.

D. The Takefman Reference (Ex. 1007)

Takefman discloses a system including a computer processing unit ("CPU") a memory module, and memory bus connecting the CPU and the memory module, as well as a co-processing unit (or input/output device). Ex. 1007, 1:48-55. The memory bus also connects the co-processing unit to the CPU. *Id.* As Takefman describes, the I/O buses that typically connect co-processors to the computer system can "create communications bottlenecks for I/O or co-processing applications." *Id.*, 1:32-38. As a result, Takefman interfaces the co-processors via the main memory system. *Id.* at 1:42-44.

Thus, Takefman introduces a TeraDIMM architecture that includes a module controller ("Rush") 301, a number of DRAM devices 302, a number of data buffer ("Bolt") devices 30, a rank of non-volatile memory devices 304, an SSD controller 305, an SPD 306, and a PIC microcontroller 307. *Id.*, 5:53-6:13. In this embodiment, data flowing between the data bus and the DRAMs 302 flow exclusively through the Bolt devices 30, while commands to the DRAMs 302 flow through the Rush 301 on their way to the DRAMs 302. *Id.*, 5:53-6:13, Fig. 3..

Takefman's module controller Rush 301 includes per-lane delay compensation circuits that allow for programmable launch times and lane de-skew on receive from the data buffers (Bolt devices 30). *Id.* 6:14-26. The specification teaches that such values "may be calibrated during manufacturing and stored in onboard memory." *Id.* However, there is no discussion for Takefman's data buffers (Bolt devices 30) to include any delay compensation circuit let alone to obtain timing information based on signals received by the Bolt devices 30.

III. LEVEL OF ORDINARY SKILL

While Patent Owner disputes Petitioners' definition of the level of a person of ordinary skill in the art ("POSITA"), resolution of such dispute is not necessary for the Board to make a determination regarding institution. Patent Owner reserves the right to further address Petitioners' improper POSITA definition in subsequent filings, if necessary.

IV. CLAIM CONSTRUCTION

The '608 Patent's challenged claims are to be construed "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b)." 37 C.F.R. § 42.100(b) (Nov. 13, 2018). The Petition does not seek construction of any terms in the '608 Patent. For purposes of this filing, Patent Owner does not propose that the Board construe any claims, but Patent Owner reserves the right to do so in subsequent filings, if necessary.

V. LEGAL STANDARDS

A. Standard for Granting an IPR

The Board may only authorize an IPR be instituted where "the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). The petitioner bears the burden of showing that the statutory threshold is met. Office Patent Trial Practice Guide, 77 FED. REG. 48,756 (Aug. 14, 2012). A petition must provide "[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent." 37 C.F.R. § 42.22(a)(2).

B. Obviousness Standard

"A patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole

would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int'l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, Case IPR2012-00001, Paper 15, at 15 (P.T.A.B. Jan. 9, 2013) (refusing to institute IPR under § 103 where the prior art did not disclose all claim limitations).

Obviousness is resolved based on factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

The conclusion of obviousness based on a combination of references must be supported with an explicit analysis of a reason to combine those references. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Such reasons must be more than "mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

VI. PETITIONER FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD OF PREVAILING ON GROUND 1

A. Petitioners fail to provide evidence that Osanai discloses "*wherein the data path corresponding to the each data signal line includes . . . a delay circuit configured to delay a signal through the data path*" (claims 1 and 4).

Claim 1 the '608 Patent defines the claimed "*data path corresponding to each data signal line*" as including "*a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals*." Ex. 1001, cl. 1. As explained in detail below, Petitioners wholly fail to offer proof that Osanai discloses each limitation of the "*delay circuit*" element. Therefore, Petitioners' Ground 1 cannot support institution.[1]

To show that Osanai satisfies the "*delay circuit*" element of the '608 Patent, Petitioners must (1) identify a claimed "*delay circuit*" in Osanai, (2) show that the "*delay circuit*" is "*include[d]*" in the claimed "*data path*," (3) show that the "*delay circuit*" is "*configured to delay a signal through the data path*," (4) show that such "*delay*" is "*by an amount determined by the command processing circuit*," and (5)

[1] Because Claim 1 is the '608 Patent's only independent claim, Osanai's failure to disclose the claimed "*delay circuit*" element also precludes anticipation of Claim 4 by Osanai.

show that such "*determin[ation]*" is "*in response to at least one of the module control signals*." Ex. 1001, cl. 1. Because Petitioners wholly fail to allege that each of these limitations in claim 1 is disclosed in Osanai, the Petition is facially deficient.

1. Petitioners do not identify a "*delay circuit configured to delay a signal*."

First, Petitioners fail to clearly identify any claimed "*delay circuit configured to delay a signal*," departing from their use of explanatory parentheticals with italicized claim language to identify other claim elements purportedly disclosed by Osanai.[2] Under the subsection "Delay Circuit," Petitioners discuss delays purportedly attributable the write leveling circuitry 322, but never expressly identify the write leveling circuitry 322 as the claimed "*delay circuit configured to delay a signal*." Pet., 43-44. Petitioners also make a passing reference to the fact that "[a]

[2] For other claim elements, Petitioners specifically and expressly identify which component(s) in Osanai purportedly satisfy the claim element. *See* Pet., 24 (identifying data connectors 120 and 130 as the "*edge connections*"); *id.*, 26 (identifying command/address/control register buffer 400 as the "*module control device*"); *id.*, 29 (identifying memory chips 200 as "*memory devices*"); *id.*, 33 (identifying data register buffers 300 as "*buffer circuits*"); *id.*, 38 (identifying data register control circuit 320 and DLL Circuit 310 collectively as the "*command processing circuit*").

similar read leveling process results in signals being delayed" but do not provide any substantive discussion of how read leveling circuitry 323 satisfies the totality of the "*delay circuit*" claim limitation. *Id.*, 43. Similarly, Petitioners reference the purported functionality of DLL Circuit 310, but fail to expressly identify Osanai's DLL Circuit 310 as disclosing the claimed "*delay circuit*" or assert that it delays any signal "*through*" any "*data path*." *Id.*

2. Petitioners do not identify where in the claimed "*data path*" any "*delay circuit*" is "*include[d].*"

Nor do Petitioners identify the claimed "*data path corresponding to each data signal line*" that "*include[s]*" any "*delay circuit"* allegedly disclosed in Osanai. Petitioners devote only a single sentence to this portion of the claim language: "To correct this timing error, the write leveling circuitry 322 delays the output timing of the DQS sent from the data register buffer 300, thus creating DQS-Post ('*delay[ing] a signal through the data path by an amount determined by the command processing circuit*')." *Id.*, 43 (emphasis in original). Petitioners and their expert offer no further explanation, wholly failing to identify any "*data path*" that "*include[s]*" Osanai's write leveling circuitry 322. This renders Petitioners' proof for this claim element deficient. *See A123 Sys., LLC v. Long Hua Technology Co., LTD.*, Case IPR2021-00894, Paper 12, at *18 (P.T.A.B. Oct. 18, 2021) (denying institution where Petitioner failed to show where in the cited reference each claim element was disclosed).

3. Petitioners do not identify a "*signal*" that is "*delay[ed]*" "*through the data path*."

Moreover, the sole "*signal*" that Petitioners point to as purportedly being "*delay[ed]*" is the "DQS sent from data register buffer 300." *Id.* Petitioners do not even attempt to show that the DQS signal sent from data register buffer 300 is delayed "*through the data path*" as the claims require, or through any data path at all. *Id.* Petitioners do not allege or demonstrate that the DQS signal traverses a "*data path*" through which it could be "*delayed*." Neither Patent Owner nor the Board should be forced to "play archaeologist with the record" to ascertain Petitioners' arguments. *See General Access Solutions, Ltd. v. Sprint Spectrum L.P.*, 811 F. App'x 654, 657 (Fed. Cir. May 11, 2020) (explaining that the prohibition on incorporation by reference prevents the Board from being forced to "play archeologist with the record" and search for arguments that might have been made outside of the parties' briefing) (citation omitted) (unpublished).

Petitioners also summarily state that "the write leveling circuitry 322 delays the output timing of the DQS sent from data register buffer 300," but fail to show how the DQS signal is actually "*delay[ed]*" by write leveling circuitry 322 as required by the claims.

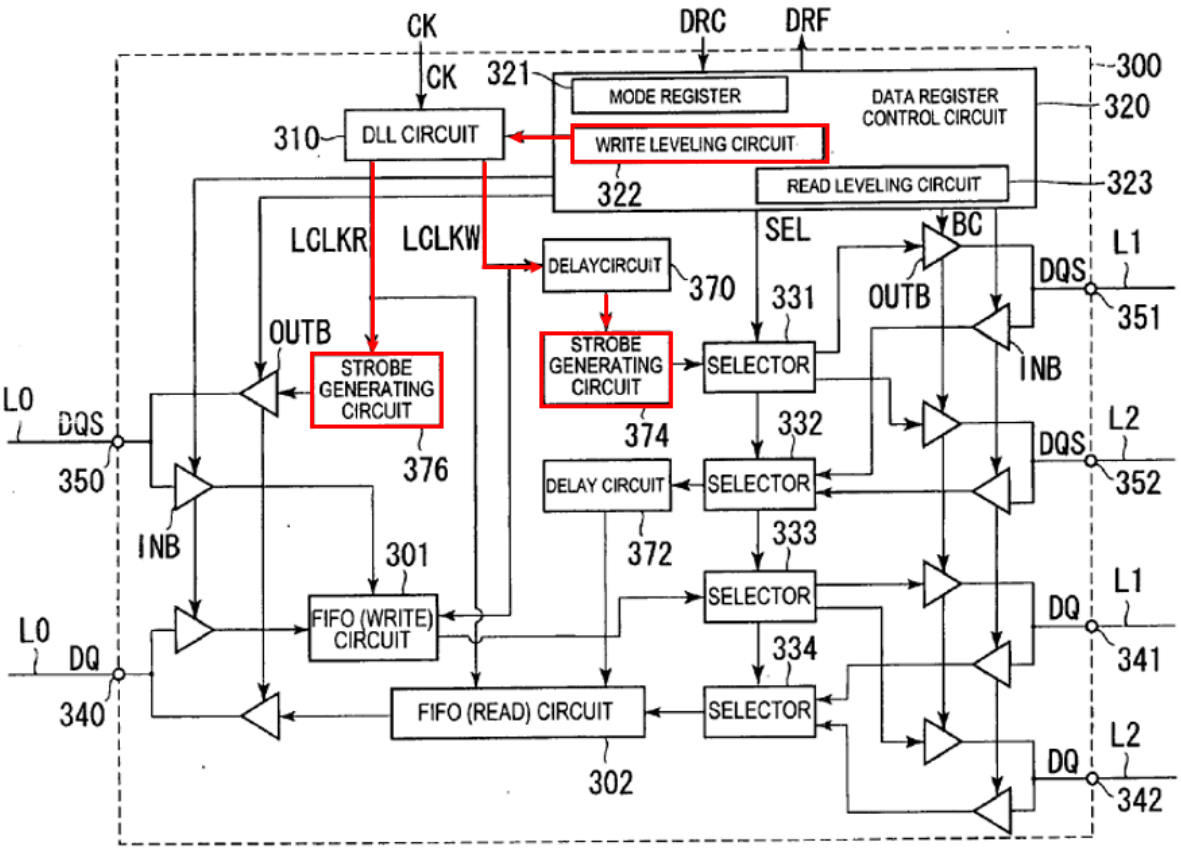


FIG.5

As shown in Osanai's Figure 5 above, Osanai's DQS signals are generated by strobe generating circuit 374 and strobe generating circuit 376. The strobe generating circuit 376 uses internal clock signal LCLKR to generate the DQS used in read operations. Ex. 1005, Fig. 5; *see also id.*, [0094] ("A strobe generating circuit 376 generates a data strobe signal DQS to be supplied to the data connectors 120, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310."). The strobe generating circuit 374 uses internal clock signal LCKLW phase adjusted a fixed 90 degrees by delay circuit 370 to generate the DQS for write operations. *Id.*; *see also id.*, [0094] ("A strobe generating circuit 374 generates a data

strobe signal DQS to be supplied to the memory chip 200, in synchronization with an internal clock LCLKW that is generated by the DLL circuit 310."). Figure 5 makes clear that any action or "*delay*" performed by write leveling circuit 322 would necessarily occur ***before*** the DQS signals are even generated by either strobe generating circuit 376 or strobe generating circuit 374. And a signal cannot be *"delay[ed]*" as claimed unless it exists. Thus, Petitioners do not show how write leveling circuit 322 is "*configured to delay*" the DQS signal "*through the data path.*"

These are threshold failures of proof that prevent Petitioners from establishing that Osanai discloses each and every limitation of claim 1 of the '608 Patent. *See Therasense, Inc. v. Becton, Dickinson & Co.*, 593 F.3d 1325, 1332 (Fed. Cir. 2010) ("Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention arranged as in the claim."). Ground 1 of the Petition fails for this reason.

VII. PETITIONER FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD OF PREVAILING ON GROUND 2

In Ground 2, Petitioners assert that Tokuhiro also satisfies the claimed "*delay*" element. Pet., 45-49. However, Petitioners cannot show—and do not even attempt to show—that Tokuhiro teaches that any delay of a signal through a data path is determined "*in response to . . . at least one of the module control signals*." In fact,

Petitioners do not show that Tokuhiro teaches any "*module control signal*" at all. For this reason, Ground 2 fails on its face.[3]

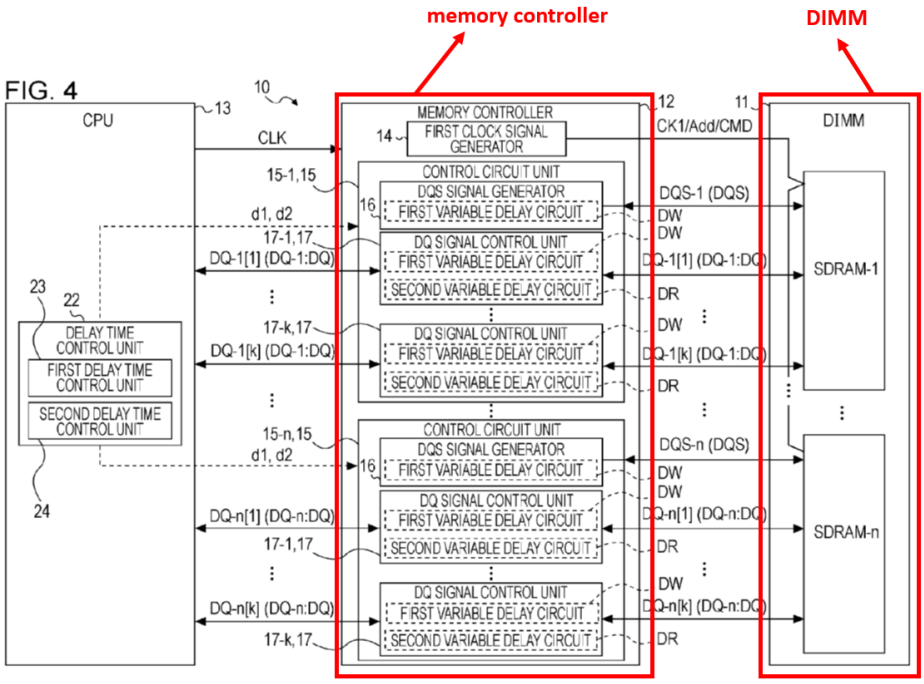
A. Petitioners fail to provide evidence that Tokuhiro discloses "*delay[ing] a signal through the data path by an amount determined . . . in response to at least one of the module control signals*" (claims 1-5).

Claim 1 of the '608 Patent (and all dependent claims) discloses a memory module with a plurality of buffer circuits that must include "*a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit* ***in response to at least one of the module control signals***." Ex. 1001, cl. 1 (emphasis added). The claims require that the "*module control signals*" are output by the module control device to the buffer circuits. *Id.* (comprising "*a module control device . . . configured to . . . output module control signals in response to the system command signals*" and "*a plurality of buffer circuits . . . configured to receive the module control signals*"). In other words, the '608 claims recite that the claimed delay circuit within the buffer circuits delays a signal through the data path in response to module control signals sent to the buffer circuits from the module control device.

[3] As Claim 1 is the '608 Patent's only independent claim, Tokuhiro's failure to disclose the claimed "delay circuit" element precludes obviousness of Claims 2-5 by a combination of Osanai and Tokuhiro, as well.

In Ground 2, Petitioners argue that Tokuhiro satisfies the claimed "*delay*" element. Pet., 45-49. Specifically, Petitioners point to Tokuhiro's write leveling technique and assert that, pursuant to such write leveling functionality, Tokuhiro "discloses calculating a second delay time for the read operation based on the first delay time determined by the write level operation." Pet., 46.

However, claim 1 of the '608 Patent requires that the delay of the claimed signal must be determined in response to at least one "*module control signal*." Ex. 1001, cl. 1. Petitioners do not show that Tokuhiro discloses any "*module control signal*," let alone that a delay circuit delays a signal through the claimed data path by an amount determined ***in response to*** any "*module control signal*." Ex. 1001, cl. 1. Moreover, the '608 claims require that the "*module control signals*" must be sent to the buffer circuits by the claimed "*module control device*," which must be "*mounted on the module board*." *Id.* Tokuhiro, however, fails to teach any such "*module control device*" because none of Tokuhiro's write leveling functionality is located on the memory module (DIMM 11) with the SDRAM memory devices:



See Ex. 1006, Fig. 4.

In other words, the configuration taught by Tokuhiro—a fly-by topology for wiring between the memory controller 12 and the SDRAM devices mounted on DIMM module 11—is fundamentally different from the memory module taught in the '608 Patent. This is because the memory module taught in the '608 Patent includes a "*module control device*" that is responsive to system command signals and a system clock signal from a system "*memory controller*," and the system memory controller is ***distinct and separate*** from the "*module control device*" that is mounted on the memory module along with the memory devices and buffer circuits. *See* Ex. 1001, Figs. 2C and 2D. Accordingly, Tokuhiro cannot teach any "*module control signals*" output from a "*module control device*" to the claimed "*buffer*

circuits"; Tokuhiro does not teach any "*module control device*" or signals that are transmitted from an on-module control device to on-module buffer circuits, as claimed. *See* Ex. 1006, Fig. 4.

Indeed, the "control signals" in Tokuhiro that Petitioner identifies as allegedly satisfying the "*delay*" claim language are "control signals d1" output from the first delay time control unit 23 to the first variable delay circuits, as well as second control signals d2 output from the second delay time control unit 24 to the second variable delay circuits. Pet., 47-48. Tokuhiro's first delay time control unit 23 and second delay time control unit 24 are located on the CPU 13, while the variable delay circuits are part of the control circuit units on the memory controller 12. *See* Ex. 1006, Fig. 4. These signals neither originate from a "*module control device*" mounted on the memory module, nor are transmitted to a "*buffer circuit*" mounted on the memory module. Rather, these signals flow from Tokuhiro's CPU to the off-module system memory controller 12, and thus cannot be the claimed "*module control signals*." Thus, Tokuhiro does not teach any claimed "*module control signals*" output from a "*module control device*" to the "*buffer circuits*." Nor does Tokuhiro teach that any delay in connection with Tokuhiro's write leveling functionality is determined "*in response to at least one of the module control signals*."

Because Petitioners cannot tenably point to any disclosure in Tokuhiro to satisfy the "*in response to at least one of the module control signals*" requirement, they employ carefully arranged ellipses to avoid the word "*module*":

Pet., iii. The claims do not merely require that the amount of delay be determined in response to "control signals"; they must be "***module*** *control signals*" output by a *"module control device . . . in response to system command signals*." Ex. 1001, cl. 1 (emphasis added). Because Tokuhiro does not teach that the delay times obtained for read and write operations are determined in response to a "*module control signal*" sent from a "*module control device*" to the "*buffer circuits*," Ground 2 fails. Ex. 1001, cl. 1.

B. Petitioners have not relied on any "*module control signal*" disclosed in Osanai for Ground 2, so the Board may not consider whether Osanai teaches one.

Petitioners have failed to demonstrate that Osanai discloses a "*delay circuit configured to delay a signal through the data path,*" and, as a result, cannot show that Osanai anticipates any claim in the '608 Patent. *See supra* Section VII.A. In Ground 2, Petitioners appear to rely on Osanai's general disclosure of a "*delay*

circuit" and a "*command processing circuit*," pointing to Tokuhiro to allegedly satisfy the remaining claim language: "*delay[ing] a signal through the data path by an amount determined . . . in response to at least one of the module control signals*." *See* Pet., 45. Indeed, Petitioners expressly state that, "[t]o the extent that Netlist argues Osanai does not explicitly disclose to '*delay a signal through the data path by an amount determined… in response to at least one of the module control signals*,' this feature is rendered obvious by Tokuhiro." *Id.* (emphasis in original). But, as described above, Tokuhiro does not teach any "*module control signals*," so Ground 2 fails. *See supra* Section VII.A.

To the extent that Petitioners intended to rely on any portions of Osanai to satisfy the claims' requirement that the amount of delay be "*determined . . . in response to at least one of the module control signals*," they have not done so. *Id.; see Sirona Dental Sys. v. Institut Straumann AG*, 892 F.3d 1349, 1356 (Fed. Cir. 2018) (It would "not be proper for the Board to deviate from the grounds in the petition and raise its own obviousness theory."). Instead, Petitioners expressly assert that Tokuhiro teaches this element, while tacitly acknowledging that Tokuhiro does not teach any "***module*** *control signal*," as evidenced by Petitioners' creative use of ellipses to omit the word "module" in certain portions of the Petition. *Id.* (emphasis added). The Board cannot credit Petitioners with arguments they did not expressly make; rather, the Board must "evaluate the Petition's arguments as presented." *See*

Universal Imaging Indus., LLC v. Lexmark Int'l, Inc., Case IPR2019-01381, 2020 WL 582147, at *9 (P.T.A.B. Feb. 3, 2020) (citing *In re Magnum Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016)).

And even if the Board was permitted to address the merits of such a combination of Osanai and Tokuhiro—one that purportedly includes a delay determined by Tokuhiro's write leveling circuitry in response to Osanai's "*module control signals*"[4]—Petitioners do not describe such a combination. "The burden rests with Petitioner to explain and prove that a person of ordinary skill in the art would have modified the asserted references in the manner proposed by Petition." *Arcelormittal v. Array Tech., Inc.*, Case IPR2018-00801, 2019 WL 4877350, at *11 (P.T.A.B. Oct. 2, 2019) ("[T]he Petition must explain the way in which the elements would allegedly be brought together to achieve the claimed invention.") (citing 35 U.S.C. § 316(e); *Magnum Tools*, 829 F.3d at 1380–81; 35 U.S.C. § 312(a)(3); 37 C.F.R. §§ 42.22(a)(2), 37 C.F.R. § 42.104(b)(4)–(5)); *see also Yamaha Golf Car Co. v. Club Car, LLC*, Case IPR2017-02141, 2019 WL 1473077, at *13 (P.T.A.B. Apr. 2, 2019) ("Simply noting that two references are in the same field of technology says

[4] Patent Owner does not concede that Osanai discloses any "module control signals."

nothing about what one reference lacks that the other reference teaches to fill the gap.").

Here, Petitioners summarily state that a POSITA would have been motivated to incorporate Tokuhiro's leveling technique in Osanai's data register control circuit 320. *See* Pet., 49. But Petitioners fail to address how any module control signals purportedly taught by Osanai would be received by Tokuhiro's write leveling circuitry—which is inside Tokuhiro's system memory controller 12, not on the memory module as in Osanai. *See* Ex. 1005 at Fig. 7, [0094], [0105], [0112]-[0113]; Ex. 1006 at 5:65-67 ("[T]he memory controller 12 has the write leveling function.").

Nor do Petitioners explain how any presumed combination of Osanai and Tokuhiro could otherwise render obvious the claimed "*delay circuit*" element. Specifically, Tokuhiro relates to delays performed *within* the memory controller, not a signal through the data path of a buffer circuit, as claimed. Ex. 1006 at 5:4-8, Ex. 1001, cl. 1. Further, Petitioners identify Tokuhiro's delay circuits DW and DR as variable delay circuits responsive to control signals d1 and d2, but these control signals are generated by Tokuhiro's CPU 13 and do not even reach Tokuhiro's DIMM module 11, and are thus not the claimed "*module control signals*." Pet., 47; Ex. 1006, Fig. 5, 6:61-7:3, 11:5-16. Petitioners have defaulted on their obligation to identify a proposed combination of Osanai and Tokuhiro that discloses the claimed elements of the '608 Patent.

"[W]ithout those structural details regarding the proposed combination," Petitioners' assertion that a POSITA could have used Tokuhiro's teaching in Osanai's data register control circuit 320 is "too thin a reed to support a conclusion of obviousness here." *Acclarent, Inc. v. Ford Albritton, IV*, Case IPR2018-00268, 2018 WL 2553983, at *6 (P.T.A.B. May 31, 2018); *see also Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1368 (Fed. Cir. 2012) ("We must still be careful not to allow hindsight reconstruction of references to reach the claimed invention without any explanation as to how or why the references would be combined to produce the claimed invention.") (internal citation omitted). In sum, Petitioners fail to provide an explanation of how Tokuhiro cures any deficiency in Osanai to create a combination that renders the claim obvious; institution should therefore be denied.

VIII. PETITIONER FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD OF PREVAILING ON GROUND 3

In Ground 3, Petitioners only rely on Takefman to satisfy the '608 Patent's claimed "*tristate buffer*" limitation. Pet., 62. Petitioners have not asserted that Takefman discloses a claimed "*delay circuit*" and are relying solely on the disclosures in Osanai and Tokuhiro to satisfy the "*delay circuit*" element. Pet., 62-63. However, as described *herein* in Sections VI and VII, neither Osanai, nor a

combination of Osanai and Tokuhiro disclose the "*delay circuit*" element. As such, Ground 3 fails for the same reasons as Grounds 1 and 2.[5] *See supra* Sections VI-VII.

IX. THE FINTIV FACTORS FAVOR DISCRETIONARY DENIAL OF INSTITUTION UNDER 35 U.S.C. § 314(a)

By the time the Board enters a final written decision in this proceeding, both parties will have spent significant time and resources resolving issues relating to the validity of the '608 Patent in the parallel district court action. The Board should exercise its discretion to deny the petition under *Fintiv I*, IPR2020-00019, Paper 11.

A. *Fintiv* Factor #1: Whether the district court granted a stay or evidence exists that one may be granted if a proceeding is instituted.

Petitioners offer no evidence that the district court would grant a stay if an IPR is instituted; indeed, Petitioners concede they "do not know if the district court will stay the case." Pet., 67. Thus, this factor is neutral. *Apple Inc. v. Fintiv, Inc.*, Case IPR2020-00019, Paper 15 at 12 (P.T.A.B. May 13, 2020) ("*Fintiv II*") (informative) (determining that Factor 1 is neutral when a stay motion has not been addressed by the district court).

[5] As Claim 1 is the '608 Patent's only independent claim, Petitioners' failure to show that either Osanai or Tokuhiro discloses the claimed "*delay circuit*" element precludes obviousness of Claims 4 and 5 by a combination of Osanai, Tokuhiro, and Takefman, as well.

B. *Fintiv* Factor #2: Proximity of the district court's trial date to the Board's projected statutory deadline for a final written decision.

As *Fintiv* explains, "[i]f the court's trial date is at or around the same time as the projected statutory deadline ***or even significantly after the projected statutory deadline***, the decision whether to institute will likely implicate other factors discussed herein . . ." *Fintiv I*, Paper 11 at 9 (emphasis added). Here, no trial date has been set in the district court action. Pet., 67. Thus, this factor is neutral, and the decision to institute should implicate the other *Fintiv* factors. At most, this factor should only have a "slight" impact on the overall determination. *See Taiwan Semiconductor Mfg. Co., Ltd. v. Fraunhofer Gesellschaft Zur Forerderung Der Angewandten Forchung Ev*, Case IPR2020-01669, 2021 WL 14332363, at *11 (P.T.A.B. Apr. 15, 2021) ("Because it is unclear whether the trial will occur before, contemporaneously with, or after the final written decision, this factor weighs slightly against exercising our discretion to deny the Petition.").

C. *Fintiv* Factor #3: Investment in the parallel proceeding by the district court and the parties at the time of the institution decision.

Petitioners predicted, without basis, that "the [district] court is unlikely to invest any resources on the grounds raised in this petition, either before or after the scheduled institution date." Pet., 67. Petitioners are wrong on several counts. After this Petition was filed, the district court ordered four rounds of claim construction briefing, set a tutorial for May 12, 2022, and ordered a claim construction hearing to

also commence May 12, 2022. Ex. 2003. These claim construction briefings, tutorial, and hearing specifically address the '608 Patent and several disputed terms from claims asserted in both the parallel litigation and challenged in the instant Petition. *See* Ex. 2004, Joint Claim Construction Chart (Apr. 14, 2022). It is also worth noting that the parties have already expended extensive resources preparing voluminous infringement contentions and invalidity contentions and references. Ex. 2005.

The institution deadline for this proceeding is July 25, 2022. By that time, the parties and the district court will have expended significant additional resources, having reviewed and digested the multiple rounds of claim construction briefing, and having concluded the tutorial and claim construction hearing on May 12, 2022. Given the approximately two and one-half months between the May 12th claim construction hearing and the July 25th institution deadline, it is reasonable to presume that the district court will issue its claim construction decision prior to the institution deadline, and Petitioners have provided no evidence or argument to indicate otherwise. The completion of the claim construction process at the district court is an objective indication of the advanced stage of the parallel litigation that favors denial of institution. *See Fintiv I*, Paper 11 at 10. ("[D]istrict court claim construction orders may indicate that the court and parties have invested sufficient time in the parallel proceeding to favor denial.").

Moreover, when considering this third factor, *Fintiv* directs the Board to consider not only the investment of the parties and the court, but also whether "the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted." *See Fintiv I*, Paper 11 at 11. Here, Petitioners failed to act diligently in filing their IPR petitions. Specifically, Patent Owner filed its complaints alleging patent infringement of four patents against Petitioners on April 28, 2021. Ex. 2006. Petitioners, however, waited eight months to file the first set of IPR petitions against the '035 and '608 Patents on December 23, 2021. *See* IPR2022-00236 and -00237. Petitioners then filed another IPR petition approximately a month later against U.S. Patent No. 8,301,833 on January 14, 2022. *See* IPR 2022-00418. Petitioners then filed two more IPR petitions on January 14, 2022—more than eleven months after the filing of Patent Owner's complaints—challenging the claims in U.S. Patent No. 10,489,314. *See* IPR2022-00744 and -00745. Overall, Petitioners lacked diligence in filing their IPR petitions against Patent Owner, which increased the investment of time and resources by the court and parties in the parallel district court proceedings. *See Fintiv I*, Paper 11 at 11. ("[N]otwithstanding that a defendant has one year to file a petition, it may impose unfair costs to a patent owner if the petitioner… waits until the district court trial has progressed significantly before filing a petition at the Office.")

Factor 3 therefore weighs in favor of exercising discretionary denial of institution.

D. *Fintiv* Factor #4: Overlap and potential conflict between issues raised in the petition and in the parallel district court proceeding.

As the Board found in *Fintiv*, "if the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial." *Fintiv I*, IPR2020-00019, Paper 11 at 12. Here, Petitioners have asserted the exact same references against every asserted claim in the parallel litigation. Thus, there is substantial overlap in the claims, grounds, arguments, and evidence. *See* Ex. 2007, Defendants' Preliminary Invalidity Contentions at 21 (Nov. 5, 2021) (generally asserting obviousness combinations including Osanai, Tokuhiro, and Takefman).

Petitioners argue incomplete overlap of issues due to their Petition addressing three claims not asserted in the parallel litigation. Pet., 66. However, the Board has recognized that "if a petition involves the same prior art challenges but challenges claims in addition to those that are challenged in the district court, it may still be inefficient to proceed because the district court may resolve validity of enough overlapping claims to resolve key issues in the petition." *Fintiv I*, Paper 11 at 13. More importantly, Petitioners' argument fails because any challenge involving non-overlapping claims depends on the dissimilarity of the claims challenged in the petition to those at issue in the district court, and Petitioners did not argue the

dissimilarity of the three non-overlapping claims. *Id., citing Next Caller, Inc. v. TrustID, Inc.,* Case IPR2019-00961, Paper 10 at 14 (P.T.A.B. Oct. 16, 2019) (denying institution even though two petitions jointly involve all claims of patent and district court involves only a subset of claims because the claims all are directed to the same subject matter and petitioner does not argue that the non-overlapping claims differ significantly in some way). All claims at issue in the Petition are generally directed to a memory module. Accordingly, the district court litigation and this Petition present the same or substantially same claims, grounds, arguments, and therefore favors discretionary denial.

Petitioners separately argue that this fourth factor "strongly favors institution" because they stipulated not to pursue invalidity on the same grounds in the litigation if the Board institutes trial in this proceeding. Pet., 66. However, the breadth of the stipulation affects the weight given in the discretionary denial analysis. For example, a petitioner stipulating not to pursue the "same grounds" presented in a petition only marginally favors not exercising discretionary denial, while a petitioner stipulating not to pursue "any ground raised or that could have been raised" weighs strongly in favor of not exercising discretionary denial. *Sand Revolution LLC v. Continental Intermodal Group-Trucking II, LLC*, Case IPR2019-01393, Paper 24, 11-12 (P.T.A.B. Jun. 16, 2020) (informative); *Sotera Wireless, Inc. v. Masimo Corp.*, Case IPR 2020-01019, Paper 12, 18-19 (P.T.A.B. Dec. 1, 2020) (precedential as to § II.A).

Here, Petitioners have not stipulated that they will not raise grounds in the litigation that "could have been raised" in the Petition. Rather, Petitioners have only disclaimed assertion of grounds involving the three particular references asserted in the Petition. Ex. 1016. Moreover, Petitioners expressly reserved the right to rely on Osanai, Tokuhiro, and Takefman with respect to "other issues" in the district court matter, such as, among other things, for background information or to support claim construction and non-infringement arguments. *Id*. at 2. Thus, potential overlap in arguments and evidence still remain despite Petitioners' (limited) stipulation. Therefore, this factor is neutral in determining whether to deny institution. *See e.g., Apple Inc. v. Pinn, Inc*., PGR2020-00066, 2020 WL 7233481, at *9 (P.T.A.B. Dec. 8, 2020) (viewing Factor 4 as neutral given some remaining overlap in arguments and evidence even after submission of limiting stipulation by Petitioner).

E. *Fintiv* Factor #5: Whether the petitioner and the defendant in the parallel district court proceeding are the same party.

As in *Fintiv*, this factor weighs in favor of denial because Petitioners and defendants in the parallel district court proceeding are one and the same. *Fintiv I*, Paper 11 at 11.

F. *Fintiv* Factor #6: Other circumstances that impact the Board's exercise of discretion, including the merits.

As explained in greater detail above, the Board should deny institution of this proceeding because Petitioners have not demonstrated a reasonable likelihood of

success due to fatal, facial flaws in the Petition. *See Fintiv I*, Paper 11 at 15 ("if the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present.").

* * *

In consideration of the totality of the above factors, the Board should exercise discretion to deny institution under the *Fintiv* decision.

X. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests the Board deny Petitioners' request for IPR of U.S. Patent No. 10,268,608.

Dated: April 25, 2022

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CERTIFICATE OF WORD COUNT

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the Microsoft Office word count for the foregoing Patent Owner's Preliminary Response Under 35 U.S.C. § 313 and 37 C.F.R. § 42.107, excluding the table of contents, table of authorities, claim listing, certificate of word count, and certificate of service, totals 7,728 words, which is less than the 14,000 words allowed under 37 C.F.R. § 42.24(b)(1).

Dated: April 25, 2022

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served on the counsel for Petitioner a true and correct copy of the foregoing Patent Owner's Preliminary Response Under 35 U.S.C. § 313 and 37 C.F.R. § 42.107, by electronic means on April 25, 2022, by delivering a copy via electronic mail to the attorneys of record for the Petitioners as follows:

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